**Amendments to the Claims:**

This Listing of Claims, as below, will replace all prior versions of claims in the present application:

**Listing of Claims:**

What is claimed is:

1. (Currently Amended) A circuit comprising:

a controller for generating first rotate up and rotate down signals for phase adjusts in a receiver link to adapt to frequency offsets, the first rotate up and rotate down signals causing rotation of a phase of a clock signal up or down to compensate for the frequency offsets; and

an adjust circuit coupled to the controller, the adjust circuit for detecting trends in the first rotate up and rotate down signals, and using combinatorial logic to adapt the first rotate up and rotate down signals for the phase adjusts based on accumulated data accumulated by an adder [[, and]] by generating second rotate up and rotate down signals improving a rate of compensation for the frequency offsets by the phase adjusts, the improvement relative to the compensation provided by using only the first rotate up and rotate down signals for adapting to the frequency offsets.

2. (Canceled)

3. (Currently Amended) The circuit of claim [[2]] 1 wherein the adjust circuit monitors for an overflow of the first rotate up and rotate down signals.

4. (Previously presented) The circuit of claim 3 wherein the adjust circuit monitors for an overflow by counting and accumulating the first rotate up and rotate down signals.

5. (Currently amended) The circuit of claim 3 wherein the adjust circuit monitors for an overflow with an up/down counter coupled to [[an]] the adder.

6. (Previously presented) The circuit of claim 5 wherein the adjust circuit generates the second rotate up and rotate down signals through detection of overflow and underflow in the adder and logically combines by the combinatorial logic the overflow and underflow with the first rotate up and rotate down signals.

7. (Previously presented) A circuit comprising:

an up/down counter for counting signals from a phase rotator control for phase adjustments by a clock-data-recovery loop of a serial receiver; and

an adder coupled to the up/down counter that outputs accumulated data indicative of a trend in the phase adjustments.

8. (Original) The circuit of claim 7 wherein the signals comprise rotate up and rotate down signals.

9. (Currently Amended) ~~A circuit comprising:~~

~~an up/down counter for counting signals for phase adjustments by a clock-data-recovery loop of a serial receiver, wherein the signals comprise rotate up and rotate down signals;~~

~~an adder coupled to the up/down counter that outputs accumulated data indicative of a trend in the phase adjustments; and,~~

The circuit of claim 8 further comprising combinatorial logic coupled to the adder to adapt the rotate up and rotate down signals based on the accumulated data.

10. (Original) The circuit of claim 9 wherein the combinatorial logic generates a new rotate up signal based on an overflow in the adder.

11. (Original) The circuit of claim 9 wherein the combinatorial logic generates a new rotate down signal based on an underflow in the adder.

12. (Original) The circuit of claim 8 wherein the adder accumulates a chosen number of most significant bits of the rotate up and rotate down signals.

13. (Previously presented) A method comprising:

monitoring trends of phase adjusts of signals from a phase rotator control of a clock-data-recovery circuit to a reference clock of a serial receiver; and

adapting the phase adjusts to create future adjusts based on previous adjusts.

14. (Original) The method of claim 13 wherein the step of monitoring further comprises utilizing an up-down counter and an adder to accumulate phase adjust data from the phase adjusts.

15. (Currently Amended) ~~A method comprising:~~

~~monitoring trends of phase adjusts of a clock-data-recovery circuit to a reference clock of a serial receiver including utilizing an up-down counter and an adder to accumulate phase adjust data from the phase adjusts, and,~~

~~adapting the phase adjusts to create future adjusts based on previous adjusts,~~ ~~including~~ The method of claim 14 further comprising utilizing combinatorial logic to generate the future adjusts based on the accumulated phase adjust data and the previous adjusts.

16. (new) The method of claim 15 wherein the phase adjusts further comprise rotate up and rotate down signals for phase rotation in the clock-data-recovery circuit, and wherein utilizing the combinatorial logic includes generating a new rotate up signal based on an overflow in the adder.

17. (new) The circuit of claim 16 wherein utilizing the combinatorial logic includes generating a new rotate down signal based on an underflow in the adder.

18. (new) The circuit of claim 14 wherein the phase adjusts further comprise rotate up and rotate down signals for phase rotation in the clock-data-recovery circuit, and wherein the adder accumulates a chosen number of most significant bits of the rotate up and rotate down signals.

19. (new) A circuit comprising:

a controller for generating first rotate up and first rotate down signals for phase adjusts in a receiver link to adapt to frequency offsets; and

an adjust circuit coupled to the controller, the adjust circuit for detecting trends in the signals, and using combinatorial logic to adapt the signals based on accumulated data [[, and]] by generating second rotate up and second rotate down signals improving a rate of compensation for the frequency offsets by the phase adjusts, and wherein the adjust circuit monitors for an overflow of the first rotate up and rotate down signals.

20. (new) The circuit of claim 19 wherein the adjust circuit monitors for an overflow by counting and accumulating the first rotate up and rotate down signals.

21. (new) The circuit of claim 19 wherein the adjust circuit monitors for an overflow with an up/down counter coupled to an adder.

22. (new) The circuit of claim 21 wherein the adjust circuit generates the second rotate up and rotate down signals through detection of overflow and underflow in the adder and logically combines by the combinatorial logic the overflow and underflow with the first rotate up and rotate down signals.

23. (new) The circuit of claim 9 wherein the rotate up and rotate down signals are first rotate up and rotate down signals for phase adjusts in a receiver link to adapt to frequency offsets and causing rotation of a phase of a clock signal up or down to compensate for the frequency offsets, and wherein the combinatorial logic outputs second rotate up and rotate down signals which improve a rate of compensation for the frequency offsets by the phase adjusts, the improvement relative to the compensation provided by using only the first rotate up and rotate down signals for adapting to the frequency offsets.